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High Performance and Low Power Modified Radix-2^5 FFT Architecture For High Rate WPAN Application

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Abstract- **This paper presents a high speed and low complexity modified radix-2^5 512-point Fast Fourier transform (FFT) architecture using an eight data-path pipelined approach for high rate wireless personal area network applications. A novel modified radix-2^5 FFT algorithm that reduces the hardware complexity is proposed. This method can reduce the number of complex multiplications and the size of the twiddle factor memory. It also uses a complex constant multiplier instead of a complex Booth multiplier. The results demonstrate that the total gate count of the proposed FFT architecture is17201. Furthermore the highest throughput rate is up to 2.4GS/s at 300MH.**

Keywords- Fast Fourier transform (FFT), modified radix-2^5, orthogonal frequency-division multiplexing (OFDM), wireless personal area network (WPAN)

I. INTRODUCTION

With the ever increasing demand for multimedia applications using wireless transmissions over short distances, the millimeter wave (mmWave) 60 GHz Wireless Personal Area Network (WPAN) has been intensively researched for many years. Currently, the IEEE 802.11 Task Group ad (IEEE 802.11ad) is developing a standard for the mmWave Wireless Local Area Network (WLAN) and WPAN systems. High rate WPAN systems will be provided for various high speed multimedia applications such as home network systems and real time video streaming services in short range indoor environments. In the PHY layer design of high rate WPANs, the Orthogonal Frequency Division Multiplexing (OFDM) modulation has been adopted, and the FFT architecture is a key component. The FFT/IFFT architecture has a high hardware complexity in the OFDM modulation of high rate WPAN systems. One OFDM symbol in the IEEE 802.11ad standards consists of a length of 512 subcarriers [1].

In recent years, there has been some research in the design of multi-path pipelined FFT architecture that provides a high throughput. Many FFT processor architectures are introduced in order to utilize the OFDM transmission, such as a Single path Delay Commutator (SDC), Multipath Delay Commutator (MDC), Single path Delay Feedback (SDF), and Multipath Delay Feedback (MDF). Among the various FFT architectures, the MDF architecture is frequently used as a solution to provide a throughput rate of more than 1 GS/s [3]–[5]. However, for applications that provide a throughput rate of over 2 GS/s, the number of data-paths can be increased to 8 or 16, which increases the hardware cost. The area becomes even larger because the memory modules are duplicated for the 16 data path approach. In order to reduce the area and power consumption, several FFT algorithms and dynamic scaling schemes have been proposed [2]–[6].

The radix of the algorithm greatly influences the architecture of the FFT architecture and the complexity of the implementation. A small radix is desirable because it results in a simple butterfly. Nevertheless, a high radix reduces the number of twiddle factor multiplications. The radix r^k algorithms simultaneously achieve a simple butterfly and a reduced number of twiddle factor multiplications [8]. The radix-2 algorithm is a well known simple algorithm for FFT processors, but it requires many complex multipliers. The radix-4 algorithm is primarily used for high data throughput FFT architectures, but requires a 4-point butterfly unit with high

complexity. Recently, radix-2^4 the FFT algorithm and architecture have been studied in order to reduce the number of complex multipliers [2], [4].In this brief, a novel modified radix-2^5 FFT algorithm and a 512-Point FFT/IFFT architecture, which can provide a high throughput of 2.4 GS /s, are proposed. The key concepts for achieving a high data throughput reduced Power and Area.

The organization of this brief is as follows. Section II describes the proposed modified radix -2^5 FFT algorithm, and Section III describes the proposed 512-point radix-2^5 FFT architecture. In Section IV describes the results. Finally, conclusions are provided in Section V.

II. MODIFIED RADIX-2 5 FFT ALGORITHM

A discrete Fourier transform (DFT) of length N is defined as follows:

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk}, k = 0,1 \dots\dots, N-1 \quad (1)$$

Where W_N is the twiddle factor and denotes the N th primitive root of unity, with its exponent evaluated modulo N .k is the frequency index and n is the time index [2]. The radix-2^k algorithm has the same butterfly structure regardless of the k value. The 512-point FFT computation with radix -2^k algorithm consists of nine arithmetic stages. The radix-2^k algorithm is formulated using k – dimensional linear index mapping. The radix-2^5algorithm can be expressed as various formulas using a common factor algorithm. The radix-2^5 algorithm is given as follows.

Applying a 6-D linear index map

$$n = \langle \frac{N}{2} n1 + \frac{N}{4} n2 + \frac{N}{8} n3 + \frac{N}{16} n4 + \frac{N}{32} n5 + n6 \rangle_N \quad ;$$

$n_1, n_2, n_3, n_4, n_5 = 0, 1$

$$n_6 = 0, \dots\dots, \frac{N}{32} - 1$$

$$k = \langle k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6 \rangle_N$$

$k_1, k_2, k_3, k_4, k_5 = 0, 1$

$$k_6 = 0, \dots\dots, \frac{N}{32} - 1. \quad (2)$$

The radix-2 ^{5}algorithm is reformulated into two decomposing methods (Method 1 and Method 2), which are called the modified radix-2 ^{5}algorithm. The common factor algorithm takes the form of

$$X(k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6)$$

$$= \sum_{n6=0}^{\frac{N}{32}-1} \sum_{n5=0}^{1} \sum_{n4=0}^{1} \sum_{n3=0}^{1} \sum_{n2=0}^{1} \sum_{n1=0}^{1} \times x\left(\frac{N}{2} n_1 + \frac{N}{4} n_2 + \frac{N}{8} n_3 + \frac{N}{16} n_4 + \frac{N}{32} n_5 + n_6\right) W_N^{nk}$$

$$= \sum_{n6=0}^{\frac{N}{32}-1} [J_{\frac{N}{32}}(n_6, k_1, k_2, k_3, k_4, k_5) \times W_N^{n_6(k_1+2k_2+4k_3+8k_4+16k_5)}] W_{\frac{N}{32}}^{n_6 k_6} \quad (3)$$

The method 1 of the modified radix-2^5 algorithm is expresses as follows:

$$= \underbrace{(-1)^{n_1 k_1}}_{\text{Stage 1 BU}} \overbrace{(-j)^{n_2 k_1}}^{\text{Stage 1TF}} \underbrace{(-1)^{n_2 k_2}}_{\text{Stage 2 BU}} \overbrace{W_8^{n_3(k_1+2k_2)}}^{\text{Stage 2 TF}}$$

$$\times \underbrace{(-1)^{n_3k_3}}_{\text{Stage 3BU}} \overbrace{W_{32}^{(2n_4+n_5)(k_1+2k_2+4k_3)}}^{\text{Stage 3TF}} \underbrace{(-1)^{n_4k_4}}_{\text{Stage 4BU}} \overbrace{(-j)^{n_5k_4}}^{\text{Stage 4TF}}$$

$$\times \underbrace{(-1)^{n_5k_5}}_{\text{Stage 5BU}} \overbrace{W_N^{n_6(k_1+2k_2+4k_3+8k_4+16k_5)}}^{\text{Stage 5TF}} W_{\frac{N}{32}}^{n_6k_6} \quad (4)$$

The common factor algorithm using other factoring method takes the form of

$$X(k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6)$$

$$= \sum_{n6=0}^{\frac{N}{32}-1} \sum_{n5=0}^{1} \sum_{n4=0}^{1} \sum_{n3=0}^{1} \sum_{n2=0}^{1} \sum_{n1=0}^{1} \times x\left(\frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + \frac{N}{16}n_4 + \frac{N}{32}n_5 + n_6\right) W_N^{nk}$$

$$\sum_{n_6=0}^{\frac{N}{32}-1} \left[K_{\frac{N}{32}}(n_6, k_1, k_2, k_3, k_4, k_5) W_{\frac{N}{16}}^{n_6k_5} \right] W_{\frac{N}{32}}^{n_6k_6} \quad (5)$$

The Method 2 of the modified radix-2^5 algorithm is expressed as follows

$$W_N^{\left(\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+\frac{N}{16}n_4+\frac{N}{32}n_5+n_6\right)(k_1+2k_2+4k_3+8k_4+16k_5+32k_6)}$$

$$\underbrace{(-1)^{n_1k_1}}_{\text{Stage 1 BU}} \overbrace{(-j)^{n_2k_1}}^{\text{Stage 1TF}} \underbrace{(-1)^{n_2k_2}}_{\text{Stage 2 BU}} \overbrace{W_{16}^{(2n_3+n_4)(k_1+2k_2)}}^{\text{Stage 2 TF}}$$

$$\times \underbrace{(-1)^{n_3k_3}}_{\text{Stage 3BU}} \overbrace{(-j)^{n_4k_3}}^{\text{Stage 3TF}} \underbrace{(-1)^{n_4k_4}}_{\text{Stage 4BU}} \overbrace{W_N^{(16n_5+n_6)(k_1+2k_2+4k_3+8k_4)}}^{\text{Stage 4TF}}$$

$$\times \underbrace{(-1)^{n_5k_5}}_{\text{Stage 5BU}} \overbrace{W_{\frac{N}{16}}^{n_6k_5}}^{\text{Stage 5TF}} \times W_{\frac{N}{32}}^{n_6k_6} \quad (6)$$

Each method has butterfly computation and twiddle factor multiplication at each stage. Equations (4) and (6) show the butterfly stages and twiddle factor multiplications of each stage. The twiddle factors W^n_{32} and W^n_{16} in (4) and (6) have complex numbers. If each radix-2^5 decomposing methods (Method 1 and Method 2) are used independently for the 512-point FFT computation, the number of twiddle factor multiplications tends to increase. However, the number of twiddle factor multiplications can be reduced by combining the Methods 1 and 2 of the modified radix-2^5 algorithm, which is called mixed method. The complex multiplication of the twiddle factors,W_{32}^n,W_{16}^n, and W_8^n , can be implemented in the canonic signed digit (CSD) constant multiplier, which contains the fewest number of non-zero digits [10]. Hence, the area and power consumption of the

complex multipliers can be reduced. The results show that the proposed FFT architecture using the mixed method of the modified radix-2^5algorithm has the lowest total normalized area of complex multipliers. Thus, it has best area efficiency as the FFT architecture.

III. PROPOSED ARCHITECTURE

In this brief, an eight parallel data-path 512-point modified radix-2^5 FFT architecture is proposed, as shown in Fig.6.There are two modules based on the modified radix-2^5 algorithm that reduce the number of twiddle factor multiplications. The first module, which consists of five processing elements (PEs), is realized using Method 1 of the modified radix-2^5algorithm, and the second module is realized using Method 2. The proposed architecture consists of butterfly units, complex Booth multipliers, complex constant multipliers, first-in first-out (FIFO), and a control unit.

A. Butterfly Units

The butterfly units perform complex additions and subtractions of two input data x[n] and x [n+n/2]. The behavior of the butterfly units is as follows. All input values are saved into the FIFO until the $N/2^{th}$ input is entered. Then, the butterfly units conduct calculations between the input values and FIFO outputs, after entering the (N/2) $+1^{st}$input. During the last clock cycles, all butterfly calculations are performed at each stage [1]. Among the butterfly outputs, the complex addition outputs are fed to the next stage. And, the complex subtraction outputs are saved in the FIFO, and then during the next clock cycles, the FIFO outputs are fed to the next stage. Butterfly unit 1 (BU1) conducts complex additions and subtractions only. However, butterfly unit 2 (BU2) includes twiddle factor multiplication utilizing the multiplexers and control signals.

B. Complex Booth Multiplier with Error Compensation

The twiddle factor multiplication is conducted using fixed width complex multipliers. The twiddle factor values stored in the read-only memory (ROM) are used as the multiplicand in the complex Booth multiplier. The modified Booth algorithm is used widely for high speed multiplications. Since the maximum clock rate of the FFT processor depends on the critical path of the complex Booth multiplier, three-level pipelined complex Booth multiplier is used for high-speed operation.

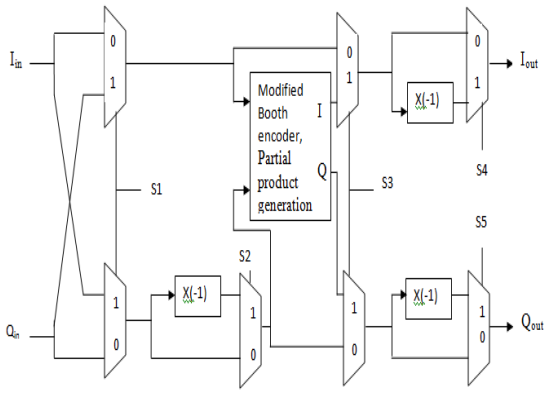

Figure 1: Block diagram of the Complex booth Multiplier

C. Complex Constant Multiplier

The proposed FFT architecture uses constant multipliers based on the can conical signed digit (CSD) representation for the complex multiplication arithmetic in stages 2, 3, and 7. The twiddle factor W_8 has only one coefficient, but twiddle factors W_{16} and W_{32}have three and seven coefficients, respectively. Mostly the existing research is using complex Booth multipliers for the twiddle factorW_{32} multiplication. However, in our design, the complex CSD constant multiplier has been used for the twiddle factor W_{32} multiplication [8]. Also, the common sub-expressions sharing (CSS) technique reduces the hardware complexity of the complex CSD constant multipliers [10], as shown in Fig.5. The constant multiplier using the CSS technique is implemented

using the common calculation patterns X1, X2, and X3. The proposed FFT processor applied CSD constant multiplier instead of complex Booth multiplier at several stages. Thus, the hardware complexity of complex multiplier is decreased by at least 54% in comparison with using complex Booth multiplier. In addition, the twiddle factor LUT size is reduced to 50% compared to the designs using the complex Booth multipliers.

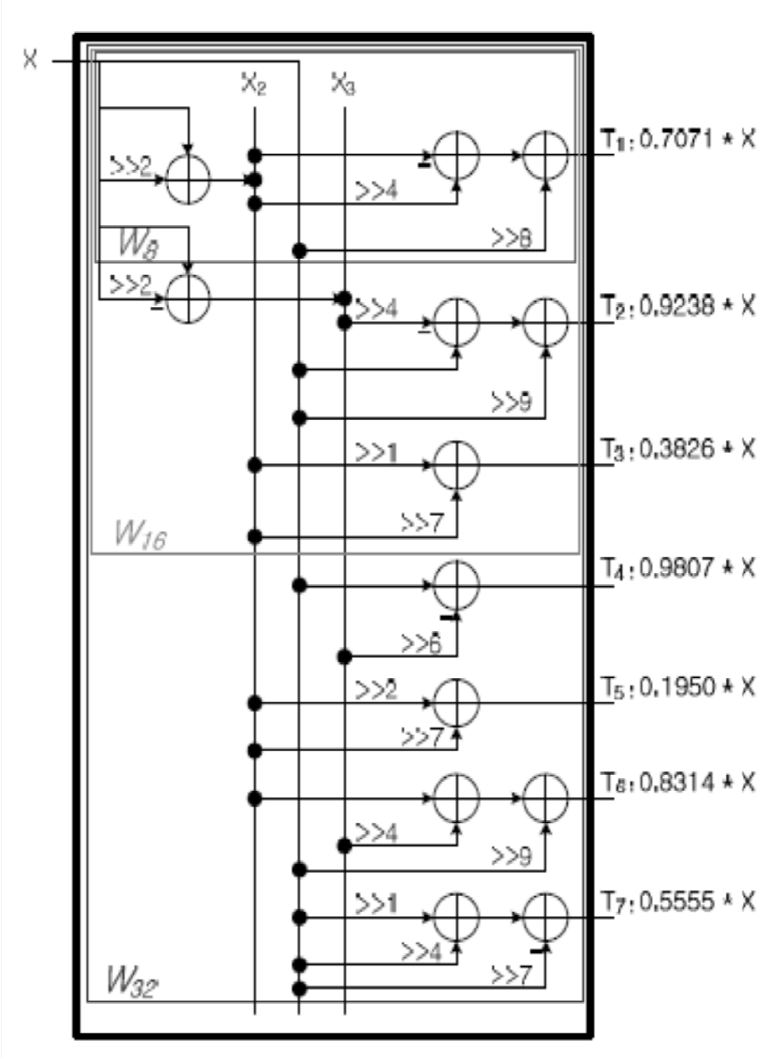

Figure 2: Block diagram of the Complex constant multiplier

IV. RESULTS

The appropriate word length and quantization error performance evaluation of the proposed FFT architecture was determined using a fixed-point simulation prior to the hardware implementation. The architecture of the proposed FFT/IFFT processor was designed in Verilog HDL and simulated to verify its functionality. Both the simulation and synthesis steps were performed using the XILINX design tool and SYNOPSYS design tool 120nm CMOS technology.

The proposed processor has 17201 gate counts and the operating clock frequency is 300 MHz The throughput rate of the proposed architecture is up to 2.4GS/s at 300 MHz, which is enough to meet the specification of IEEE 802.11ad standard. Both designs presented in [3] and [5] are 2048-point FFT processors for OFDM-based WPAN applications, which do not target the existing specific standards. Although the number of parallel data-paths in the proposed design is double than that of the four parallel 2048-point FFT architecture presented in [3], which indicates a more competitive and lower hardware complexity as compared to the conventional architectures.

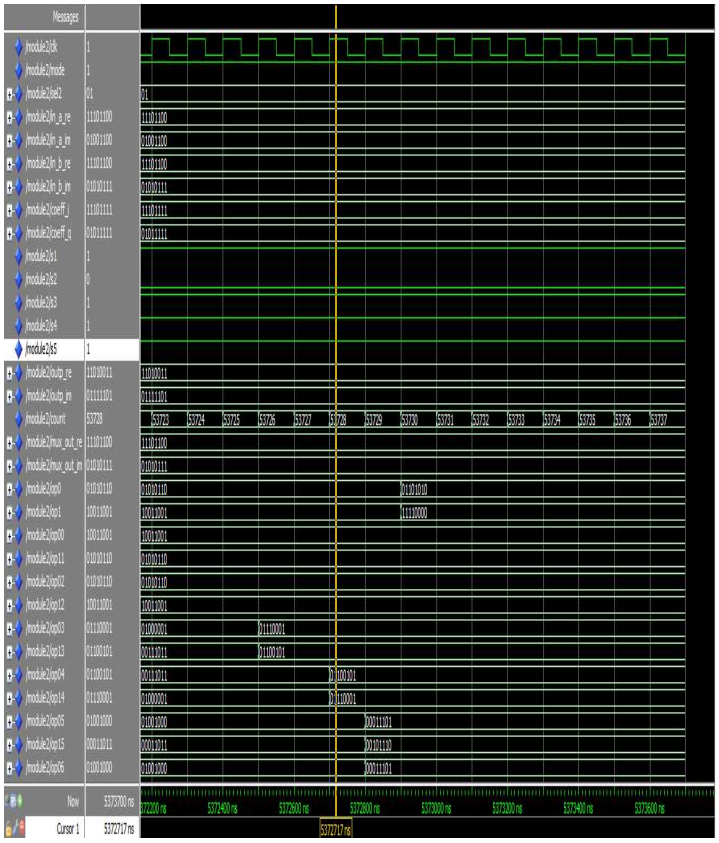

Figure 3: Simulation of the proposed eight parallel data path 512-point modified radix-2^5 FFT/IFFT architecture.

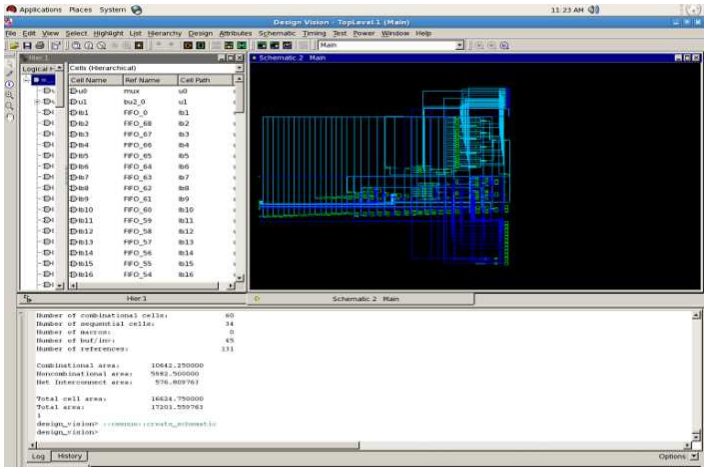

Figure 4: Simulation result of Area Report

Table I. Synthesized Area Report

S.No	Description	Area
1	Combinational area	10642.250000
2	Non-Combinational area	5982.500000
3	Net Interconnect area	576.809763
4	Total cell area	16624.750000
5	Total area	17201.559763

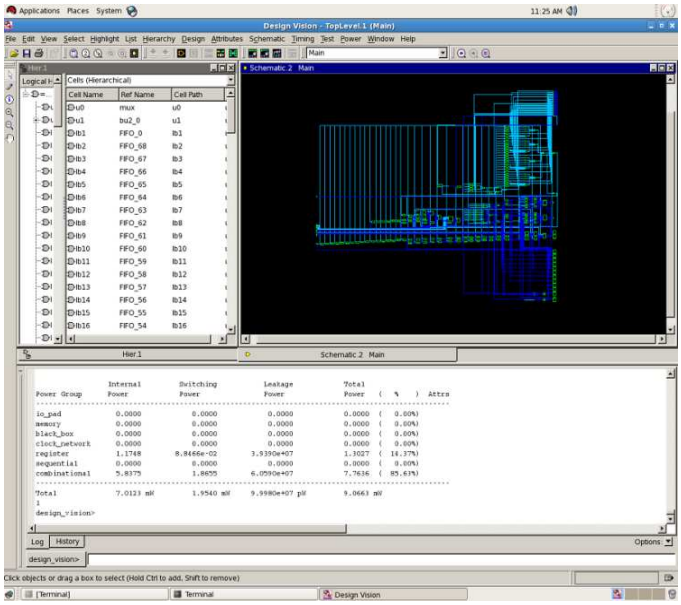

Figure 5: Simulation result of Power Report

Table II. Synthesized Power Report

S.No	Description	Area
1	Cell Internal Power	7.0123mW
2	Net Switching Power	1.9540mW
3	Total leakage Power	9.9980pW
4	Total Power	9.0663mW

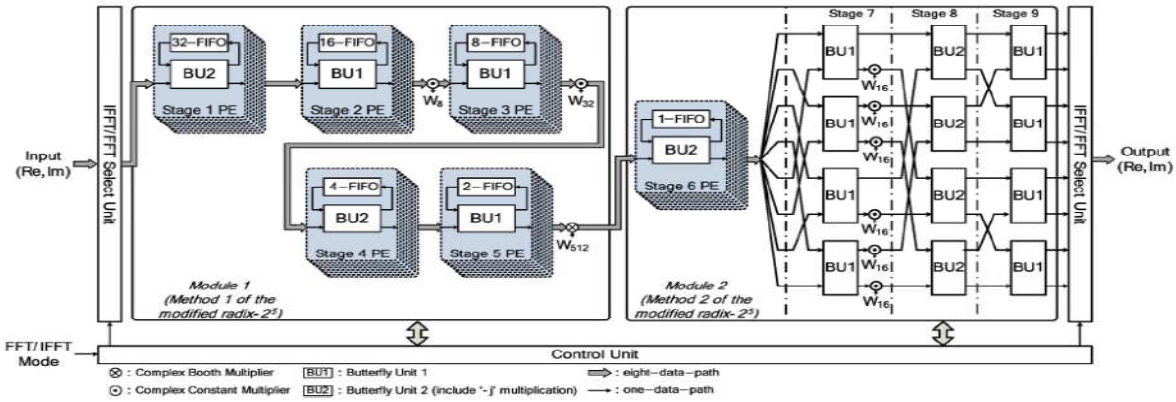

Figure 6: Block diagram of the proposed eight parallel data-path 512-point modified FFT/IFFT architecture.

Table III: Performance of The proposed FFT architecture

Parameter	Proposed	[3]	[5]
FFT size	512	2048	2048
Technology	120nm	90nm	90nm
No. of data-path	8	4	8
FFT algorithm	Modified Radix-2^5	Mixed radix	Mixed radix
Gate Count	17201	20444	21224
Architecture	MDF	MDF	MDF
Throughput	2.4GS/s	1.2	2.2
Power consumption (mW)	9.0663	45	60

V. CONCLUSION

The modified radix-2^5algorithm and the eight parallel data-path 512-point modified radix-2^5 FFT architecture have been proposed with 2.4GS/s for OFDM-based WPAN applications. The number of complex Booth multipliers and twiddle factor LUTs are reduced using the modified radix-2^5 algorithm. The proposed modified radix-2^5 FFT architecture is the most area-efficient architecture for the eight parallel 512-point MDF FFT architecture. The highest throughput rate is up to 2.4GS/s at the clock frequency of 300MHz. The proposed architecture has potential applications in high rate OFDM-based WPAN systems.

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